AMENDMENT under 37 C.F.R. § 1.111
U.S. Appln. No. 10/003,170

IN THE CLAIMS:

Please amend the claims as follows:

1. (Currently amended) An apparatus comprising:

an individual memory device including a memory array having a first portion and a second portion, the first portion of the memory array being different than the second portion of the memory array, wherein the memory array is adapted such that the first portion of the memory array is accessible only by a first processor and the second portion of the memory array is accessible only by a second processor, wherein the memory array further comprises a third portion that is different than the first portion and the second portion, the third portion of the memory array accessible by both the first processor and the second processor, and wherein the memory array is further adapted to dynamically alter a size of the first portion and the second portion of the memory array depending on an operational load of the first processor or the second processor.

2. (Cancelled)

3. (Original) The apparatus of claim 1, wherein the first portion and the second portion of the memory array are both coupled to a same clock signal.

4. (Original) The apparatus of claim 3, wherein the first portion and the second portion of the memory array are coupled to a same power supply potential.

5. (Cancelled)

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6. (Previously presented) The apparatus of claim 1, wherein the memory array is further adapted to increase the size of the first portion and decrease the size of the second portion due to an increase in the operational load of the first processor.

7. (Original) The apparatus of claim 1, wherein the memory array is further adapted such that the first processor may access the first portion of the memory array substantially simultaneously as the second processor accesses the second portion of the memory array.

8. (Original) The apparatus of claim 1, wherein the memory array is further adapted such that the first processor may read the first portion of the memory array as the second processor writes to the second portion of the memory array.

9. (Original) The apparatus of claim 1, wherein the memory array comprises memory selected from the group consisting of static random access memory, dynamic random access memory, read only memory, electrically erasable and programmable read only memory, and flash memory.

10. (Currently amended) An apparatus comprising:

~~a~~ an individual memory device including a memory array having a first portion and a second portion;

a first processor; and

a second processor, wherein the first portion of the memory array is directly accessible only by the first processor via a first bus, and the second portion of the memory array is directly accessible only by the second processor via a second bus.

11. (Cancelled).

12. (Original) The apparatus of claim 10, wherein the memory array comprises a first port and a second port, the first port coupling the first portion of the memory array to the first processor and the second port coupling the second portion of the memory array to the second processor.

13-15. (Cancelled)

16. (Original) The apparatus of claim 10, wherein the memory array comprises a third portion that is different than the first portion and the second portion, wherein the third portion of the memory array is accessible by both the first processor and the second processor.

17. (Original) The apparatus of claim 10, wherein the first portion and the second portion of the memory array are both coupled to a same clock signal and a same power supply potential.

18. (Original) The apparatus of claim 10, wherein the memory array is adapted to dynamically alter a size of the first portion and the second portion of the memory array depending on an operational load of the first processor or the second processor.

19. (Original) The apparatus of claim 10, wherein the memory array is adapted to dynamically alter a size of the first portion and the second portion of the memory array depending on an operational load of the first processor and the second processor.

20. (Original) The apparatus of claim 10, wherein the memory array is further adapted such that the first processor may access the first portion of the memory array substantially simultaneously as the second processor accesses the second portion of the memory array.

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21. (Original) The apparatus of claim 10, wherein the memory array comprises static random access memory.

22-34. (Cancelled)

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